

NASA TECHNICAL
MEMORANDUM



NASA TM X-1168

NASA TM X-1168

FACILITY FORM 602

N 66-10318	
(ACCESSION NUMBER)	
8	
(THRU)	
15	
(PAGES)	
(CODE)	
15	
(NASA CR OR TMX OR AD NUMBER)	
(CATEGORY)	

GPO PRICE \$ _____

CFSTI PRICE(S) \$ _____

Hard copy (HC) _____

Microfiche (MF) _____

ff 653 July 65

SELECTIVE ELECTROPLATING
OF ETCHED CIRCUITS

by Charles E. Whitfield, Sr., and Howard Herzog

Goddard Space Flight Center
Greenbelt, Md.

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • NOVEMBER 1965

NASA TM X-1168

**SELECTIVE ELECTROPLATING
OF ETCHED CIRCUITS**

By Charles E. Whitfield, Sr., and Howard Herzig

Goddard Space Flight Center
Greenbelt, Md.

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

For sale by the Clearinghouse for Federal Scientific and Technical Information
Springfield, Virginia 22151 - Price \$1.00

SELECTIVE ELECTROPLATING OF ETCHED CIRCUITS

by

Charles E. Whitfield, Sr. and Howard Herzog

Goddard Space Flight Center

SUMMARY

Etched copper circuit boards are commonly gold plated to prevent the copper from tarnishing. It is frequently necessary to remove the gold from the terminal pads to which components will be connected in order to achieve a reliable soldered joint. To avoid the waste of material and time involved in this removal procedure, a technique has been developed for producing boards on which only the conductive paths between terminals are gold plated, the pads themselves being plated with some more suitable metal.

Separate positive films of the conductor and terminal pad patterns are used to sequentially produce the photoresist masks required for the plating of each area with its respective metal. A negative of the entire circuit is then used to produce a new photoresist mask covering the circuit, so that the unwanted copper can be etched away.

CONTENTS

Summary	iii
INTRODUCTION	1
PROCEDURE	3
PROCESS ADVANTAGES	3
References	4

SELECTIVE ELECTROPLATING OF ETCHED CIRCUITS

by

Charles E. Whitfield, Sr. and Howard Herzig
Goddard Space Flight Center

INTRODUCTION

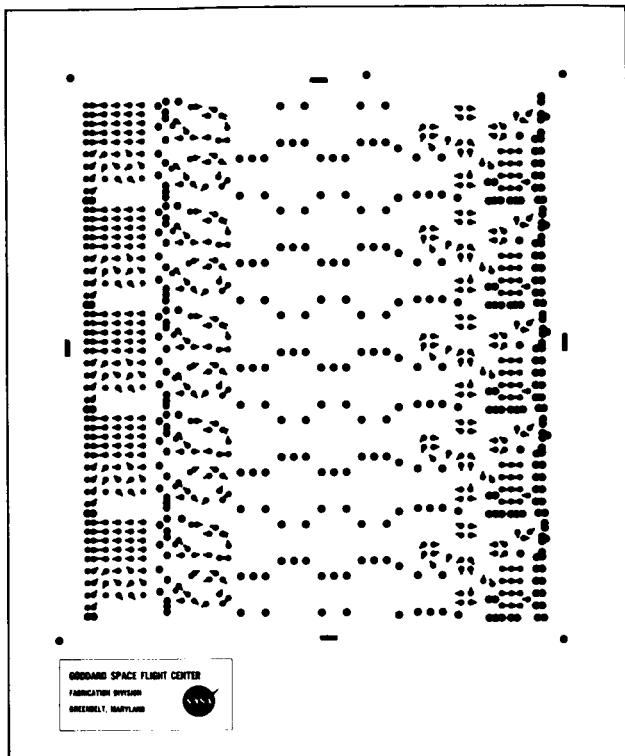
Printed circuit boards are used extensively wherever electronic circuitry is required, such as in the television, radio, telephone and aerospace industries. The techniques commonly used for producing these boards are well documented in the literature (References 1, 2, and 3).

Typically, the artwork for the entire circuit is prepared by laying out black tape on mylar film. A positive photographic print of this artwork is made on film. A copper-clad board, usually an epoxy-fiberglas laminate, is coated with a photosensitive resist, which is then allowed to dry. The resist is exposed to an arc lamp through the positive transparency. The unexposed resist, corresponding to the circuit pattern, is removed in a developer. The circuit, including the terminal pads, is gold plated to prevent the copper from tarnishing and to protect it from any corrosive environment. The hardened resist is stripped from the board and the unwanted copper is etched away using the gold as a maskant for the circuit pattern underneath.

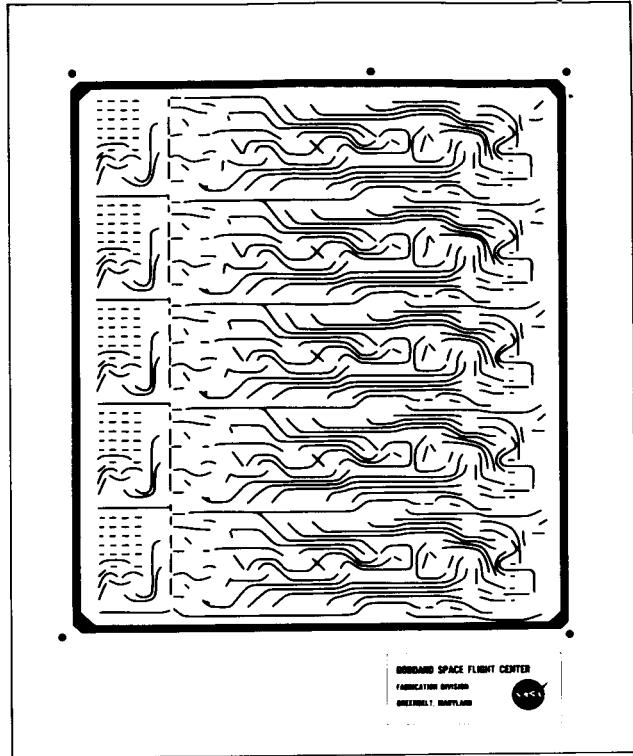
Considerable controversy has arisen as to the desirability of soldering to gold plated terminals, especially in aerospace applications, where high reliability is essential. Tests have been conducted (Reference 4) which show that the gold will dissolve in the solder to form a brittle tin-gold intermetallic compound. This is especially harmful when the gold electrodeposits exceed a thickness of 50 microinches (0.000050 in.), because the strength of the joint decreases as gold content of the gold-solder solution increases.

To avoid this problem, the gold is commonly erased from the terminal pads prior to soldering. Depending on the number of pads on a board, this operation can be both time-consuming and wasteful of gold. In addition, the circuit may be degraded by removing or abrading through the copper.

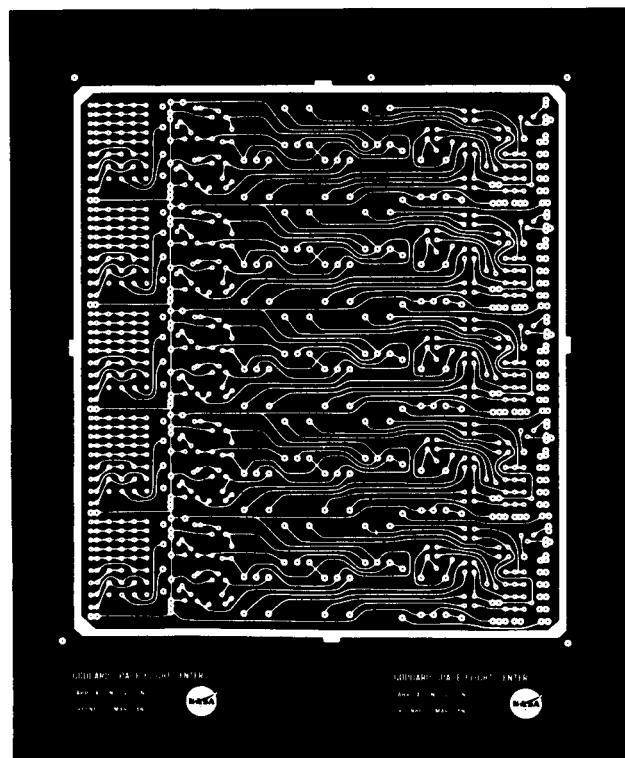
A process of selective plating, whereby the terminal pads may be plated with a material more desirable than gold, such as solder plate, has been developed and appears to be a practical approach to this problem.



(a) Positive transparency pattern for terminal pads



(b) Positive transparency pattern for conductor paths



(c) Negative transparency pattern for complete circuit

Figure 1—Typical transparencies for selective electroplating of an etched circuit.

PROCEDURE

The artwork required for this process is produced on two sheets of mylar. The terminal pads plus registration marks for aligning the subsequent films on the board are laid out on one sheet. The conductor paths plus registration marks are laid out on the second sheet. Two positive films, one of the sheet with the pads (Figure 1a) and the other of the sheet with the conductor paths (Figure 1b), are made. The two sheets of artwork are aligned and a negative of the combined circuit is prepared (Figure 1c). In order that the circuit pattern on the negative and the final board be continuous, it is necessary that the pads and conductor paths overlap slightly when the two pieces of artwork are aligned.

The three films are aligned by means of the registration marks and the alignment holes are drilled with the same template used for drilling alignment holes in the circuit board. Pins are inserted into these holes to assure alignment of the film on the board during exposure.

The board is coated with photosensitive resist and dried. The positive film of the conductor pattern is aligned on the board, the resist is exposed and developed to remove the unhardened portion and the bared copper paths are gold plated.

The hardened resist is removed from the board, which is then recoated. The positive of the terminal pad pattern is aligned on the board, exposed and developed, and the pads are then plated with the desired metal.

Again the hardened resist is removed and the board coated a third time. By exposing the board through the negative of the entire circuit, the remaining, unplated portion of the copper cladding is bared, leaving resist over the previously plated areas. The unwanted copper is then etched with ferric chloride or other suitable etchant. After etching, the hardened resist may be left on the circuit pattern until the board is ready for soldering, at which time it can be easily removed with a suitable solvent. The board is now ready for its final cleaning, after which it is trimmed and holes are drilled in the pads for component leads.

PROCESS ADVANTAGES

The above description is limited to the plating of two distinct metals on different areas of the circuit. By a simple extension of the process, as many different metals as desired can be plated on a single board. For example, it is frequently desirable to plate plug-in terminals on circuit boards with rhodium for increased wear resistance, so that it would not be uncommon for a board to have gold, solder plate and rhodium on various portions of the circuit.

The use of a last coat of resist over the plated areas during the etching process eliminates the necessity of selecting an etchant which will not attack any of the plated materials, as one is not relying on the electrodeposits themselves to act as resists. In addition, should there be pinholes in the plating, the portions of the circuit underneath the pinholes will be protected from the etchant.

REFERENCES

1. Schlabach, T. D., and Rider, D. D., *Printed and Integrated Circuitry Materials and Processes*. New York: McGraw-Hill Book Co., 1963.
2. Denstman, H., and Shultz, M. J., *Photographic Reproduction*. New York: McGraw-Hill Book Co., 1963.
3. Eastman Kodak Company, "Photosensitives Resists for Industry," First Edition, Rochester, N. Y., 1962.
4. Foster, F. G., "Embrittlement of Solder by Gold from Plated Surfaces." Special Technical Publication 319, pp. 13-20, New York: American Society for Testing Materials, January 1962.